REMARKS

Claims 16-35 are pending. In this office action, Claims 16-18, 28-30, 32-33 are rejected under 35 USC102(b) as being anticipated by US Patent No.: 6,084,259 to Kwon et al (hereinafter "Kwon"), Claims 23-27, 31 and 34-35 are rejected under 35 USC 103(a) as being unpatentable over Kwon in view of US Patent No.: 6,472,698 to Nakashiba (hereinafter "Nakashiba"), and Claims 19-22 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner is appreciated for the thoughtful examination and indication of allowable claims in the Office Action. However, the Applicant respectfully traverses the rejections and believes that Claims 16 - 35 shall be allowable over Kwon and Nakashiba, viewed singly or in combination. In the foregoing amendments to the claims, the Applicant has attempted to further clarify the distinctions of claims 16 and 28 over the cited references, which led to the corresponding amendments to the dependent claims. The amendments to the Specification correct some informalities. No new matters have been introduced. Reconsideration of the pending claims is respectfully requested in view of the amendments and flowing remarks.

As amended, Claim 16 recites:

> forming a substrate with a first layer being a first conductive type of a semiconductor material and a second layer being a second conductive type, the second layer being on top of the first layer and fully covering the first layer so as to form a junction therebetween that prevents substrate noise diffused into photo elements when a first voltage is applied to the first layer and a second voltage is applied to the second layer, wherein the junction is reversely biased, and
>
> wherein the CMOS image sensor is integrated with accessory CMOS circuits to facilitate the CMOS image sensor to operate as desired.

(*Emphasis added*)

There are at least two distinct features recited in Claim 16 that are neither taught nor suggested in Kwon. First, a junction (e.g., a PN junction) is formed between a first and a second layer on top of the first layer and fully covering the first layer. As shown in

FIG. 2 of the pending application, a (second) layer 204 is on top of the (first) 202 while the layers 202 and 204 are two different types of semiconductor material, for example, one being an N type and the other being a P type. Second, when a first power potential is applied to the substrate and a second power potential is applied to the layer, the junction is reversely biased.

Referring to FIG. 7 of Kwon, on top of the substrate 501 is a layer 502. As indicated clearly in FIG. 7, the substrate 501 is of P+ type while the layer 502 is P- type. Technically, these two types are considered as one conductive type of semiconductor material (P type), well known to those skilled in the art. In view of claim 16, the Examiner may interpret these two layers 501 and 502 being two types of semiconductor material. However, a junction simply *could not be formed* between these two layers, P- type and P+ type, and further the two layers 501 and 502 conduct when a first power potential is applied to the substrate 501 and a second power potential is applied to the layer 502.

Evidently knowing the above presented deficiency in Kwon in view of Claim 16, the Examiner interprets another layer 503 to be "*a layer on top of the substrate*" (*see*, lines 13-14 on page 2 of the Office Action). The Applicant respectfully points out that such interpretation is not supported in Kwon. As clearly shown in FIG. 7, the layer 503 is on top of the layer 502 that is on top of the substrate 501. In other words, there is a layer 502 between the layer 503 and the substrate 501. Technically, known to those skilled in the art, a junction could not be formed between the layer 503 and the substrate 501.

One of the objectives in the present invention is to overcome the noise issue by building inherently a substrate noise barrier. According to Claim 16, such substrate noise barrier is achieved by "*forming a reversely biased junction that* prevents substrate noise diffused into photo elements when a first voltage is applied to the first layer and a second voltage is applied to the second layer". Evidently, neither Kwon nor Nakashiba, viewed singly or in combination, have taught or suggested the combined features

recited in Claim 16. In fact, Kwon has taught away from Claim 16 by using an extra layer 502 between a substrate 501 and a layer 503.

Claim 28 is an apparatus claim incorporating substantially similar features recited in Claim 16. The Applicant wishes to apply the above reasons to support Claim 28. Accordingly, the Applicant submits that the combined features recited in Claim 28 are neither taught nor suggested by Lee, and the claim 28 shall be allowable over the cited references. Reconsideration of claims 28-35 is respectfully requested.

In view of the above amendments and remarks, the Applicant believes that Claims 16-35 shall be in condition for allowance over the cited references. Early and favorable action is being respectfully solicited.

The Applicant appreciates the Examiner for granting an interview to discuss Claim 16 in view of the cited references.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplementary Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned at (408)777-8873.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to "Commissioner of Patents and Trademarks, Washington, DC 20231", on Sep 27, 2004.

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Respectfully submitted;

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